Claim Amendments:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Previously Presented) A system comprising:

a data processor having an I/O buffer;

a memory having an I/O buffer coupled to the I/O buffer of the data processor, the memory storing code to control said data processor to:

determine a delay amount, wherein the delay is associated with a difference between an amount of time to process a portion of video data to amount of time to process a portion of audio data associated with the video data;

assert a transfer of processed audio data to memory through a data port;

assert, after waiting the delay amount, a transfer of a representation of the processed audio data from memory to an audio output through a data port;

a video processor to process the portion of video data to generate processed video data;

an audio processor to process the portion of audio data to generate processed audio data;

a memory controller comprising:

a first register portion to enable a transfer of the processed audio data to memory; and

a second register portion to enable a transfer of the representation of the processed audio data from memory to an audio output.

17. (Original) The system as in Claim 16, wherein said video processor further includes:

an analog video encoder to:

digitize analog video data to generate digital video data;

decode digital video data to analog video;

provide digital video data related to interlaced video data to a digital video processor;

provide the video data to the video output; and

said digital video processor to de-interlace digital video data related to interlaced video data.

18. (Original) The system as in Claim 17, wherein the digital video processor is to further process MPEG transport packets into video data.

19. (Original) The system as in Claim 16, wherein the audio processor is to further digitize analog audio data to digital audio data.

20. (Original) The system as in Claim 16, wherein the data port is coupled to the video processor.

21. (Original) The system as in Claim 16, wherein the data port is coupled to the video processor to transfer the processed audio data to and from memory.

22. (Original) The system as in Claim 16, further including a host bus interface unit, with an I/O bus coupled to the I/O bus of the data processor, to provide access to memory to the data port.

23. (Original) The system as in Claim 16, wherein the delay is determined according to a mode of operation.

24. (Original) The system as in Claim 23, wherein the mode of operation includes processing multimedia data associated with analog audio and video content to generate the portion of audio data and the portion of video data.

25. (Original) The system as in Claim 23, wherein the mode of operation includes processing multimedia data associated with digital audio and video content to generate the portion of audio data and the portion of video data.

26. (Original) The system as in Claim 23, wherein the mode of operation includes generating picture-in-picture video data by mixing multimedia data associated with digital audio and video content with video data associated with an analog video content.

27. (Original) The system as in Claim 23, wherein the mode of operation includes generating picture-in-picture video data by mixing multimedia data associated with analog audio and video content with video data associated with an analog video content.

28. (Original) The system as in Claim 16, wherein memory is to further store code to:

assign a first address associated with a first portion of memory to store processed audio data;

assigning a second address associated with a second portion of memory to read a set of a representation of the processed audio data.

29. (Original) The system as in Claim 28, wherein a rate of transfer of processed audio data is altered to keep an amount of stored data between the first and second addresses constant.

30. (Original) The system as in Claim 16, wherein the data port is a multiple channel data access port and further includes:

a first FIFO channel for transferring the processed audio data to memory; and

a second FIFO channel for transferring the representation of the processed audio data from memory.

31. (Original) The system as in Claim 30, further including a third FIFO channel for performing general functions.

32. (Original) The system as in Claim 31, wherein the first and second port include separate controls for initiating data transfers.

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)